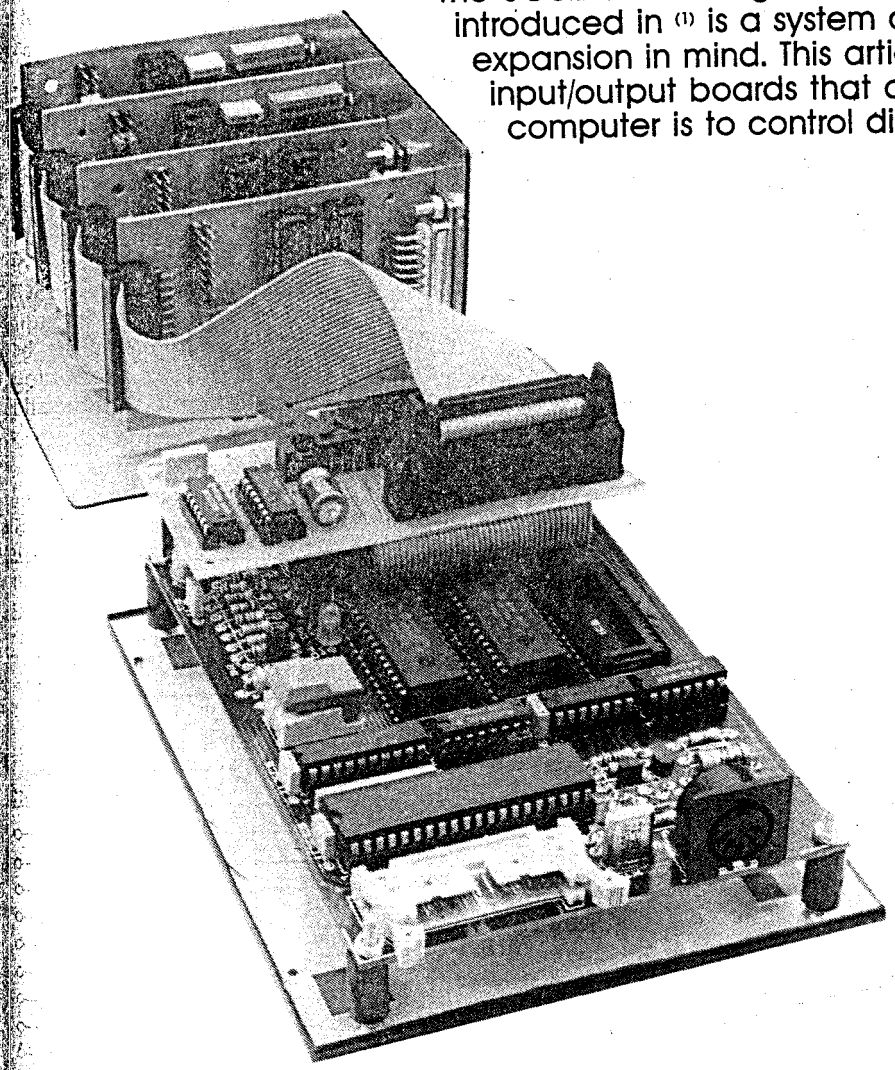
PERIPHERAL MODULES FOR BASIC COMPUTER

from an idea by J. Haudry

The 8052-based single-board process and control computer introduced in [1] is a system designed with hardware expansion in mind. This article describes two modular input/output boards that are indispensable when the BASIC computer is to control digital or analogue peripherals.



Peripheral modules for BASIC computer.

Technical characteristics:

- Modular I/O system comprises one address decoder/interface, and one or more input and/or output modules.
- Parallel mounting of up to eight digital I/O modules.
- Analogue output module based on 10-bit DAC supplies accurate voltage for control applications.
- Voltage span: 0 to 10.23 V, programmable in 10 mV steps.
- Use of one or more analogue output modules restricts the maximum number of modules controlled by 1 address decoder/interface to 7.
- Maximum of 2 address decoder/interface boards enables control of up to 16 digital I/O modules, or 14 analogue output modules.
- Power digital outputs sink up to 500 mA at 50 V. Maximum total dissipation of output driver: 2.25 W (dissipation is 0.5 W, for example, when 300 mA is supplied).

Just for those who do *not* know: the system described in reference [1] is a single-board computer based on Intel's Type 8052AH-BASIC v1.1 microcontroller. As indicated by the type number, the computer can be programmed in BASIC. Programming is done with the aid of a dumb terminal (or a host computer running a terminal emulation program), and a bidirectional RS232 link to the BASIC computer. The system can run programs from an on-board EPROM, and is, therefore, ideal for small-scale process and control applications ('turnkey' systems). Interestingly, control software is written and debugged direct on the system, and loaded into EPROM by the CPU, i.e., without the need of an EPROM programmer.

The BASIC computer has been one of the most popular projects published over the last year or so in this magazine. Users have found it simple to build, program, and connect to existing equipment. The BASIC interpreter in the 8052AH-BASIC is relatively fast, and supports a number of extremely useful bit-manipulation commands. Machine code programming is also possible when the Intel reference guide is available.

After our publishing of the 'bare bones' of the BASIC computer, many users have expressed a firm interest in input/output extensions for connection to the available bus. The modules described here are our answer to these requests. Readers may be interested to know that the modules are also compatible with a 8751-based autonomous input/output controller with RS232 interface, to be described in a forthcoming issue of this magazine.

Functional description of the I/O modules

Two types of bus-connected module are described here:

- a bidirectional digital interface with 8 inputs and 8 buffered outputs;
- an analogue output module capable of supplying a highly accurate output voltage between 0 and +10.23 V, in steps of 10 mV.

Between the BASIC computer's bus and these modules sits a simple address decoder. The I/O modules are small units, and one address decoder allows parallel connection of up to 8 digital modules, or up to 7 modules when analogue and digital types are used simultaneously. The BASIC computer itself allows the connection of a maximum of two address decoders. The modular structure of the expanded BASIC computer is illustrated in the block diagram of Fig. 1. The address decoder provides a bus in the form of a flatcable, which runs from one I/O module to the next.

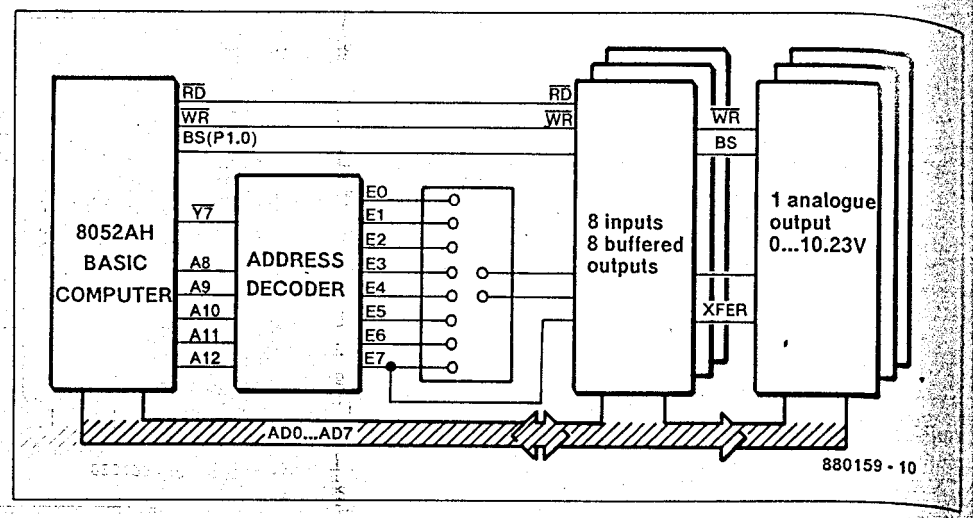


Fig. 1. The input/output system for the BASIC computer is a modular structure that gives the user freedom of configuration. The I/O boards are connected direct to the databus of the microcontroller, but are addressed in the memory segment reserved for peripheral circuits.

Address decoder for I/O modules

The circuit diagram of Fig. 2 shows the simplicity of the address decoder for the I/O modules. Monostable IC_2 is used for timing one of the control signals for the 10-bit digital-to-analogue (D-A) converter.

The presence of address lines A11 and A12 allows defining two address ranges, so that two decoders can be mounted in parallel, each with a different jumper configuration (A-D). Table 1 shows that each card occupies 256 addresses.

Address decoder IC_1 supplies 8 enable signals, $\overline{E0}$ to $\overline{E7}$. The special use of $\overline{E7}$ on the analogue output module will be reverted to, as well as the function of signal BS, which is supplied direct by the BASIC computer, and runs to the analogue output board(s) via the address decoder board.

Monostable IC_2 changes the timing of $\overline{WR}$ to provide a signal called $\overline{SWR}$

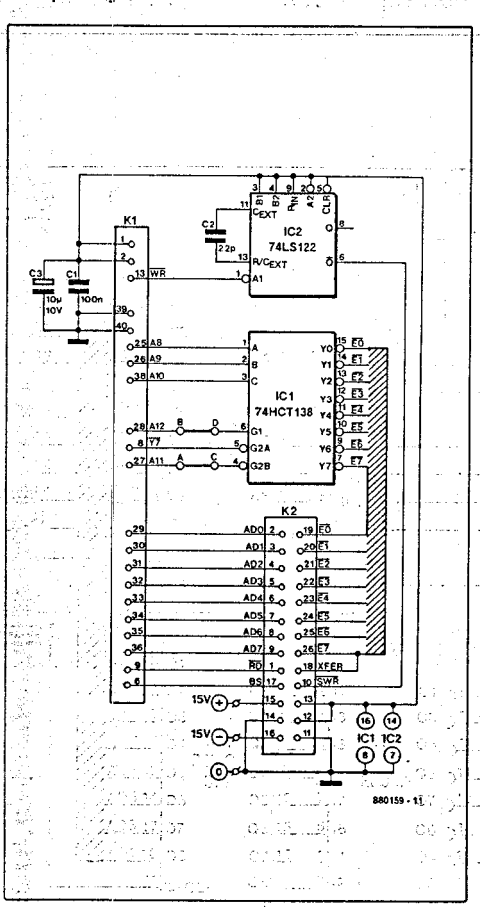


Fig. 2. The interface shared by the I/O modules is composed of an address decoder that divides the available memory space for I/O in 8 blocks of 256 addresses, and a circuit that modifies the timing of the $\overline{WR}$ pulse to ensure correct loading of the D-A converter.

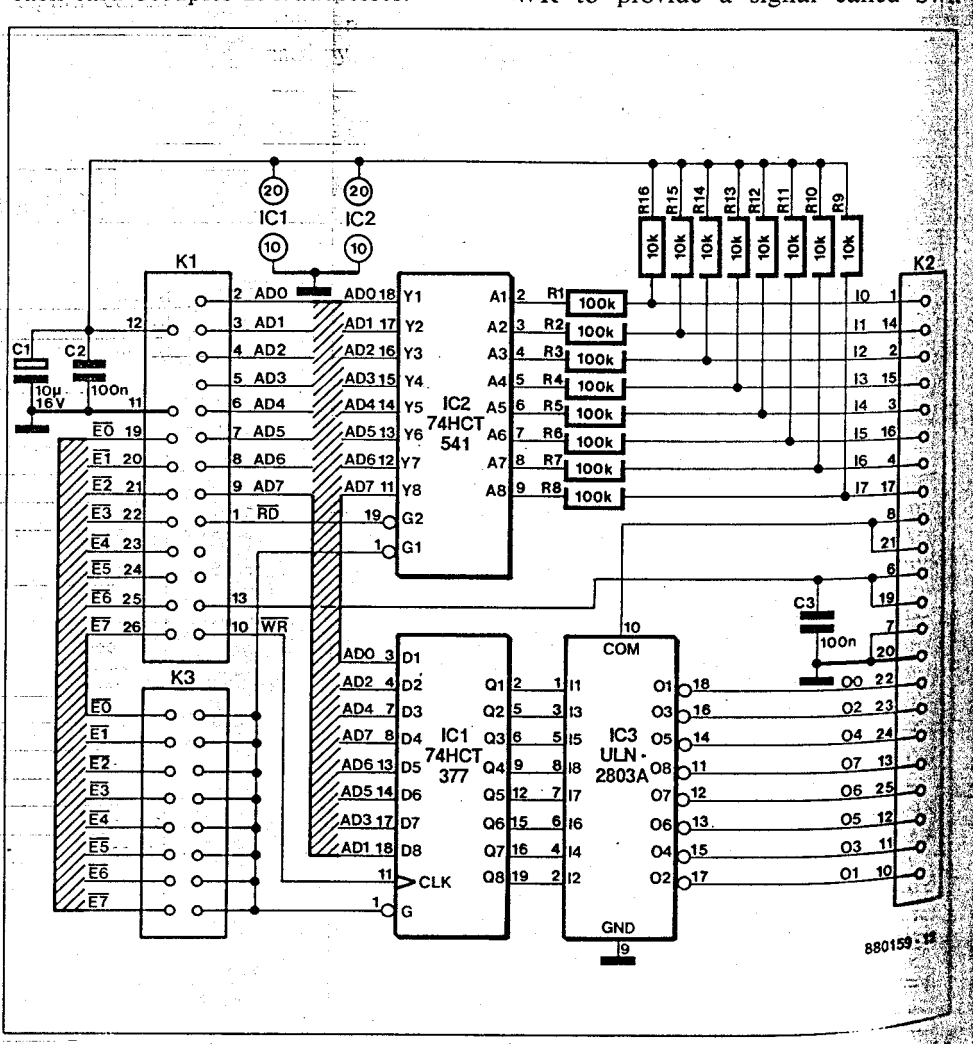


Fig. 3. Circuit diagram of the bidirectional digital interface. Up to 8 of these circuits can be controlled by a single address decoder.

short write or *special write*), needed for controlling the D-A converter on the analog output module.

Bidirectional digital input/output module

The circuit diagram of this basically simple unit is given in Fig. 3. Circuit IC_1 is an octal latch whose inputs are connected to the databus of the BASIC computer. Data is latched into IC_1 on the rising edge of the memory write signal, $\overline{WR}$, but only when input $\overline{G}$ is held logic low. This condition is satisfied when the address supplied by the computer falls within the range preset by the jumper on block K_3 (see Table 1.). When the processor writes a databyte to a digital output, e.g., at address F600H, jumper E6 should be installed on K_3, and jumpers BD and AC on the address decoder board (Fig. 2).

Circuit IC_2 is controlled by the same enable line, $\overline{Ex}$, as IC_1, and in addition by the read signal, $\overline{RD}$, of the microcontroller. As a further configuration example, jumper $\overline{E4}$ should be installed on K_3, and jumpers BC and AD on the decoder board, to enable the microcontroller to read a databyte at address EC00 on the digital I/O board. The databyte read by the selected card is formed by the logic configuration of the signals applied to inputs I0 to I7 on the 25-way D connector, K_2. Note that the input lines have pull-up resistors, so that any non-connected input is read as a logic high level. The pull-up resistors allow the digital input to be connected direct to an existing open-collector or open-drain output.

The Type ULN2803 in position IC_3 is an 8-way inverting power buffer composed of high-voltage, high-current darlington transistor arrays. This IC enables the digital output to directly control a wide range of loads, such as relays, solenoids, stepper motors and LED displays. Figures 4a and 4b show the inter-

Table 1. Address assignment of I/O modules.

Signal $\overline{Y7}$ defines address range E000...FFFF, split in two by A11 and A12. Lines A8, A9 and A10 define 8 blocks of 256 addresses.

enable signal	wire links BD and AC	wire links BC and AD
$\overline{E0}$	F000...F0FF	E800...E8FF
$\overline{E1}$	F100...F1FF	E900...E9FF
$\overline{E2}$	F200...F2FF	EA00...EAFF
$\overline{E3}$	F300...F3FF	EB00...EBFF
$\overline{E4}$	F400...F4FF	EC00...ECFF
$\overline{E5}$	F500...F5FF	ED00...EDFF
$\overline{E6}$	F600...F6FF	EE00...EEFF
$\overline{E7}$	F700...F7FF	EF00...EFFF

All addresses in hexadecimal.

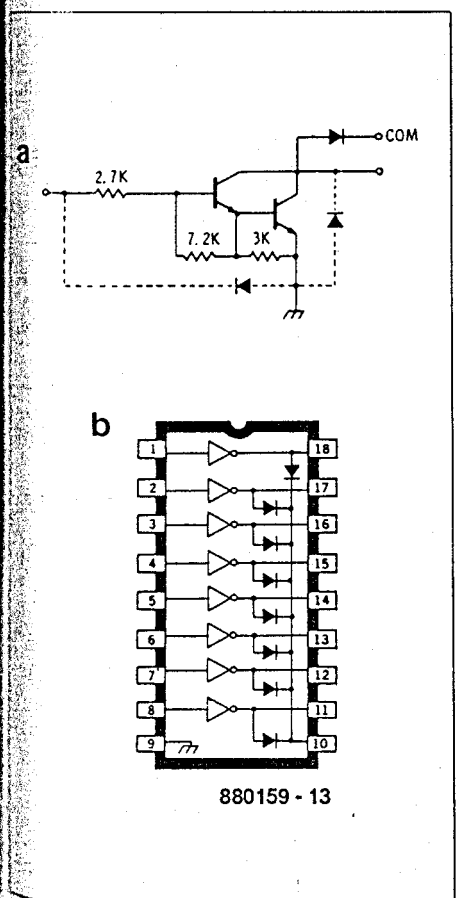


Fig. 4. Internal diagram of the ULN2803 from Sprague. Each of the 8 surge-protected darlington transistors in this chip can switch (inductive) loads of up to 500 mA.

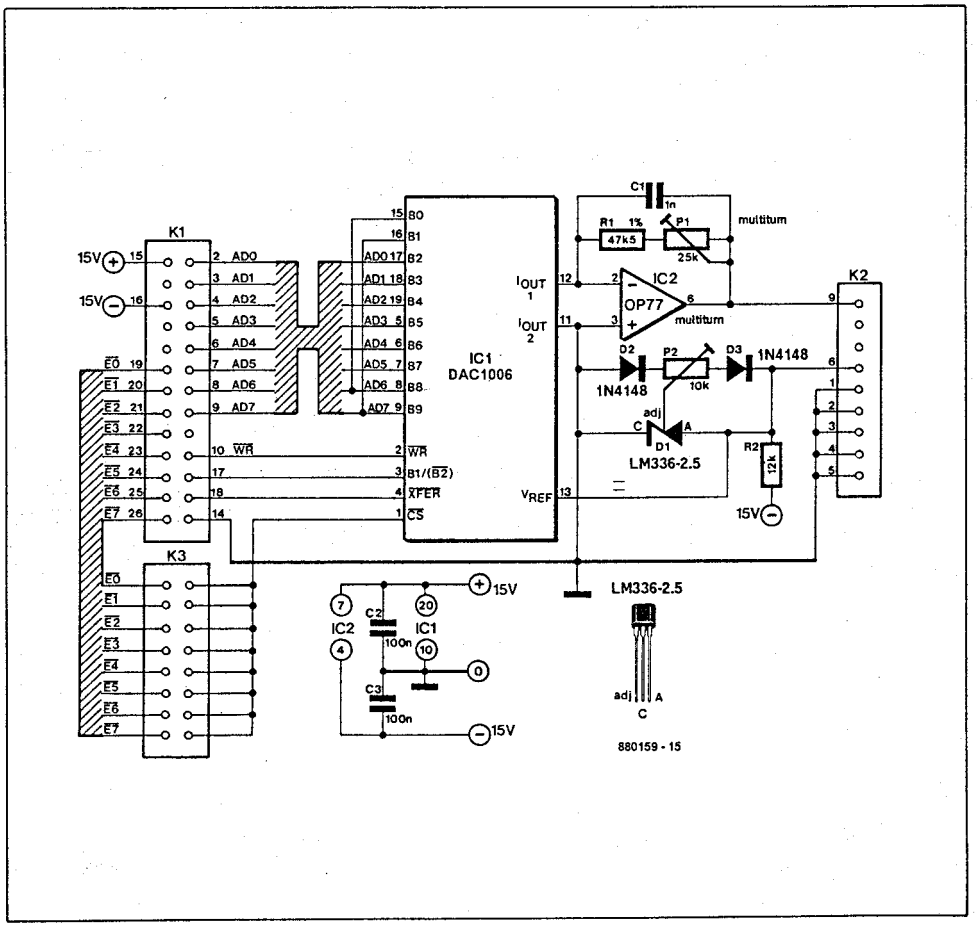


Fig. 5. The analogue output module is based around a 10-bit digital-to-analogue converter Type DAC1006 from National Semiconductor. The output voltage span is from 0 to 10.23 V in 10 mV steps.

nal structure of the ULN2803. Note that the buffers are of the inverting type, and that internal anti-surge diodes are provided to prevent damage to the open-collector output transistor when the current through the inductive load (relay coil) is interrupted. The anti-surge diodes are internally connected to a common rail, which is brought out to pin 10. This means that the supply voltage for the inductive loads controlled by the ULN2803 can be connected to pins 21 and 8 of K_2.

Analogue output module

The heart of the D-A module shown in Fig. 5 is formed by IC_1, a Type DAC1006. This 10-bit DAC is remarkable for its excellent stability and capability to be controlled from an 8-bit bus. Loading of data (0 to 1023_{10}) is done in two successive operations, under control of the logic level of the BS (byte select) signal applied to pin 3. This signal comes direct from the microcontroller 8052AH-BASIC via an output line of port P1. Users should decide for themselves which of these lines is to be used for providing signal BS.

The Type DAC1006 has a few pecularities which call for a rather special circuit configuration around it. Firstly, the DAC has a specific requirement as regards the duration of the databyte. The timing diagrams of Fig. 6 show that databytes are present on the bus for only 40 µs after the $\overline{WR}$ pulse (Fig. 6a). The DAC1006, however, requires data to be present for at least 200 ns (Fig. 6b). This problem is solved by monostable IC_2 in the address decoder circuit (Fig. 2). Note that the 74LS122 used for this purpose is not available in the HCT version.

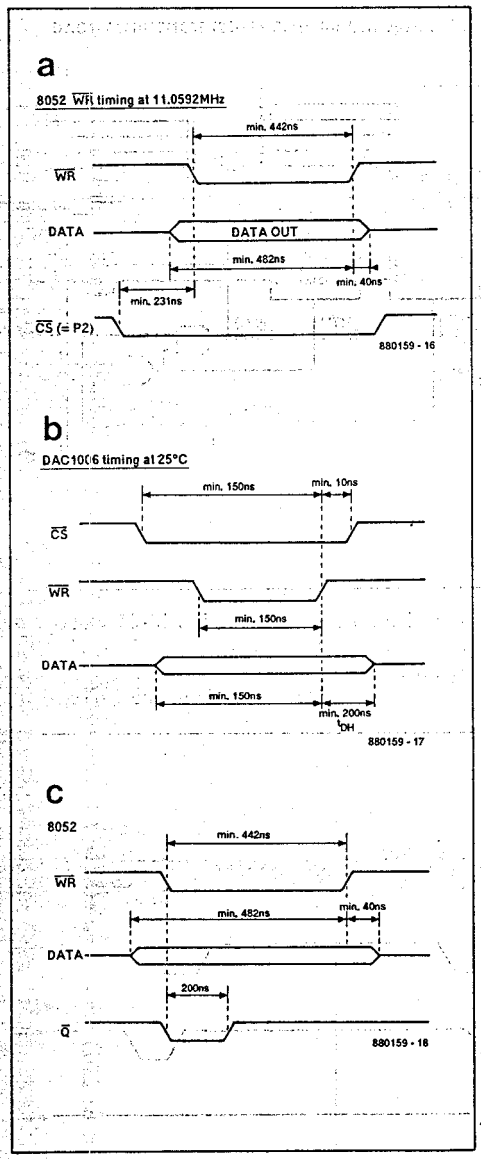


Fig. 6. For the DAC1006 to operate corectly, data should remain stable on the the databus for at least 200 ns following the rising edge of the $\overline{WR}$ pulse (Fig. 6b), which is not so on the databus of the 8052AH-BASIC (Fig. 6a; f_{CL} = 11.0592 MHz). A monostable multivibrator is, therefore, required to shorten the $\overline{WR}$ pulse (Fig. 6c).

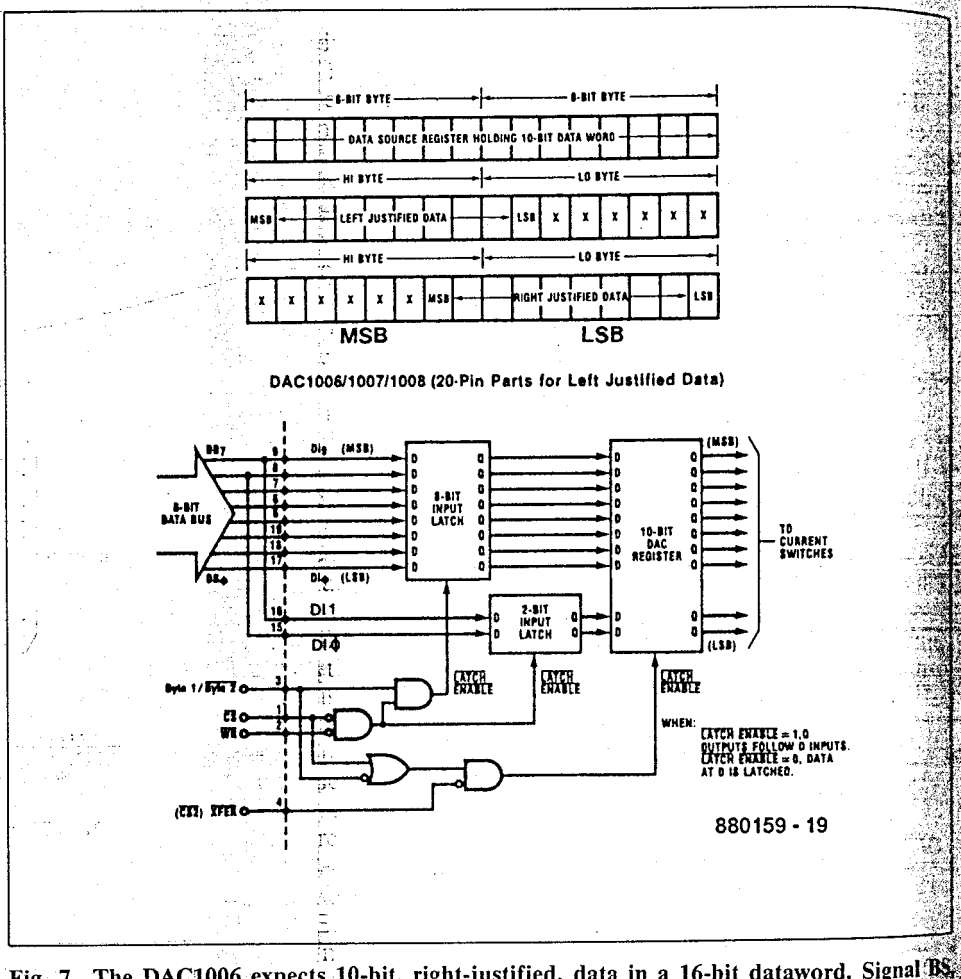


Fig. 7. The DAC1006 expects 10-bit, right-justified, data in a 16-bit dataword. Signal BS, together with $\overline{WR}$ and $\overline{CS}$, is needed to ensure that data from the 8-bit databus is sequentially latched into the device. A further signal, XFER, effects the transfer of the complete dataword from the latches to the internal conversion register.

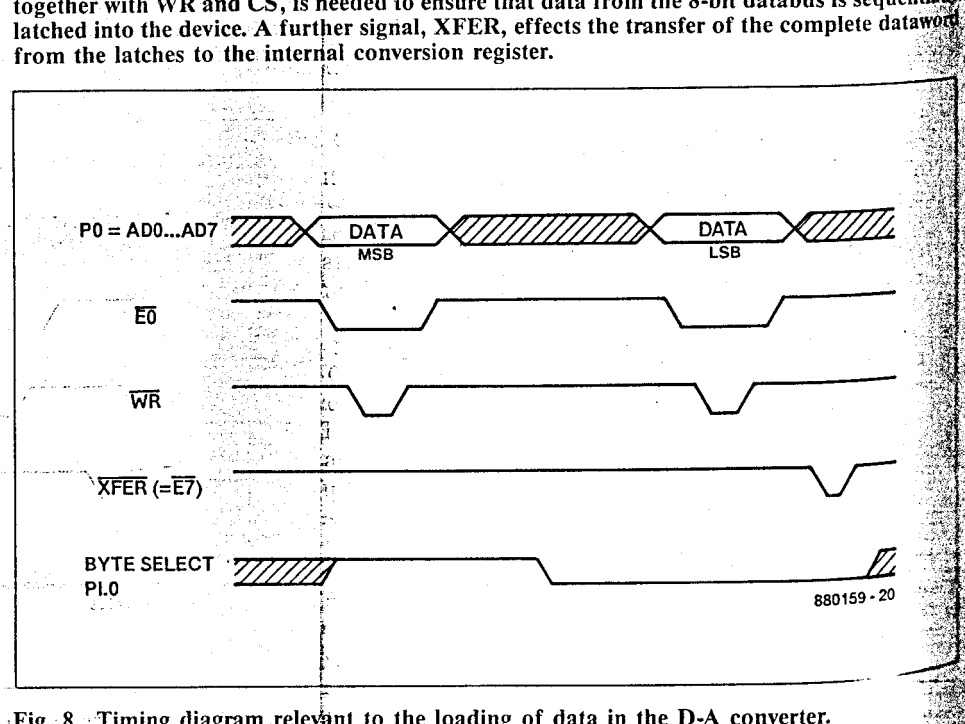


Fig. 8. Timing diagram relevant to the loading of data in the D-A converter.

ading the DAC

e se nd peculiarity of the Type C100 has to do with the way it is ded with digital data. Figure 7 shows signal BS allows the chip to latch 10-bit dataword as 8, followed by 2, Unconventionally, the 10 databits left-justified in 16 available bit lo- ions. Fortunately, in spite of the htly unusual configuration of lines 0 to AD7, and B0 to B9, it is still sible to achieve right-justified data multiplication of the right-justified ginal 10-bit data by 64. The first 8 bits loaded when BS is logic high, the 2 aining bits when BS is logic low (see Fig. 8).

ce the 10-bit dataword is available in latches, it is ready to be transferred the conversion register. This operation controlled by signal XFER, which is ply $\overline{Ex}$ supplied by the address coder board. This explains why only 7 rds can be connected to the address coder when one or more analogue put cards are being used. In that case, $\overline{E7}$ is not available for enabling a tal I/O module because it serves to k the transfer of the databits to the nversion register in the DAC1006.

gure 8 shows the time relation between signals involved. As an example, the alogue output module is addressed by while BS is provided by port line 0 of the 8052AH-BASIC.

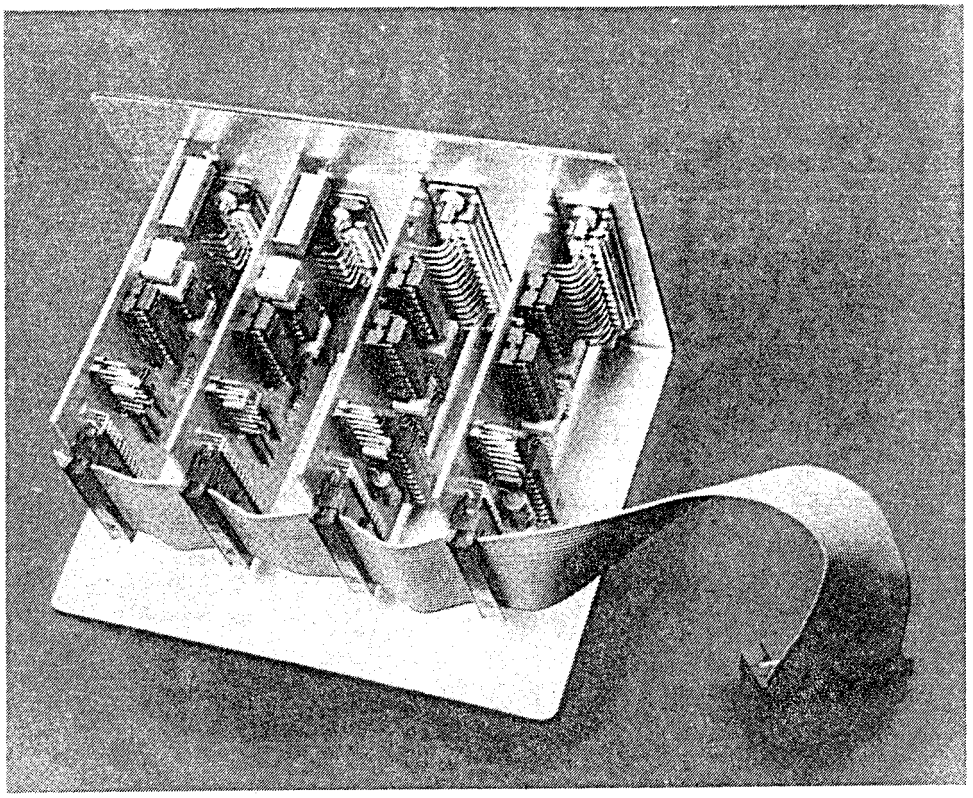
art ers may still be able to use $\overline{E7}$ addressing an eighth card, even if e or more analogue output cards are ng used. This is possible provided it is ured that the contents of the latches correct the moment the 8th card is dressed, **and** that the databyte written the latch of the selected card by $\overline{E7}$ XFER) is correct also (refer to the ng in Table 2).

e external reference voltage for the C1006 is provided by D_1, whose ther- l coefficient can be accurately com- nsated by preset P_2.

om current to voltage

e output of IC_1 supplies a current ich is converted to voltage in opamp Preset P_1 allows defining the full- le value of the output voltage. The of a relatively expensive opamp Type P-77, which achieves an offset voltage only 50 μs at an ambient temperature 25° C, may be questioned given the p size of 'only' 10 mV.

could be argued that a more common- available opamp with an external off- compensation resistor would give the e results as the OP-77. This is not so, wever, because the external compensa- n resistor would have a fixed value, ile the output resistance of the con- ter hip changes with every new ital alue loaded, due to the different nfiguration of the internal R-2R lad- network.



With reference to the simplified diagram of Fig. 9, the effect of this change on the static accuracy of the I-V converter can be expressed as the magnitude of the error voltage, calculated from

$$\text{error voltage} = V_{os}(1+R_F/R_O)$$

where R_O is a function of the digital value written to the DAC:

$R_O \approx 10$ kΩ for more than 4 logic high bits;

$R_O \approx 30$ kΩ for any single logic high bit.

Therefore, the offset gain varies as follows:

code = 001111111111:
$V_{err1} = V_{os}(1+10^4/10^4) = 2V_{os}$.

code = 010000000000:
$V_{err2} = V_{os}(1+10^4/3\times10^4) = {}^4/_3 V_{os}$.

The error difference between these values is $^2/_3 V_{os}$.

It will be evident from the above that the non-linearity of the output voltage is a function of the opamp's offset voltage. When this is low (OP-77), the maximum deviation is also low, athough still dependent of the digital value written to the DAC.

Construction and alignment

The peripheral extension modules for the BASIC computer are three printed circuit boards (Figs. 10, 11 and 12) interconnected by a bus formed by flat ribbon cable. The layout of the boards is such that the output connector, K_2, can be fitted onto the equipment front panel, with the board mounted perpendicular to this at the inside. At the other end of the cards, a 26-way flatcable plugged into K_1 runs from one card to another, connecting all of these to the bus card, which is mounted on the BASIC computer. The total length of the cable should not exceed about 30 cm to prevent digital interference on the databus.

The address decoder/interface card can be fitted direct on to the BASIC computer board, and is connected to it by a short length of flat ribbon cable. On the computer board, connect pin 7 of IC_3 (address decoding signal $\overline{Y7}$) to pin 8 of the 40-way connector (K_2). It is also necessary to choose the Port 1 line to

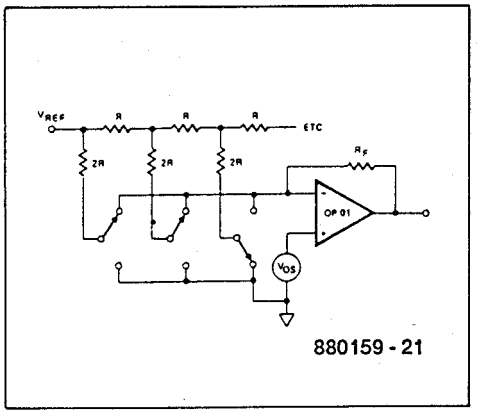
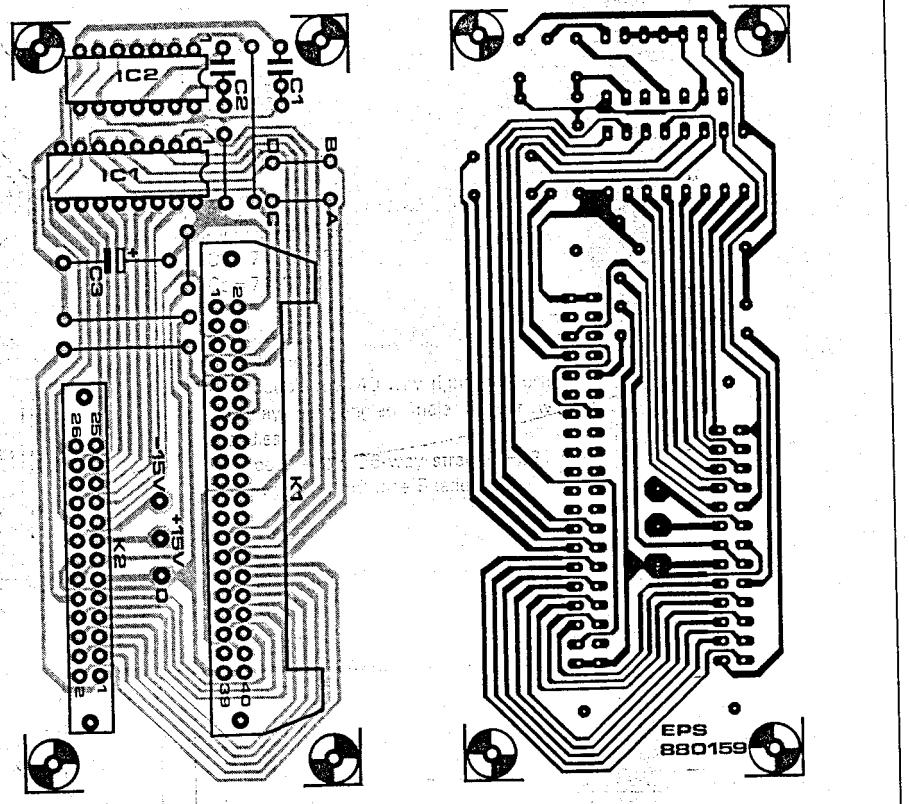


Fig. 9. Variation in output resistance of the DAC as a function of the converted code gives rise to a variable offset current at the input of the opamp, which translates current to voltage, and so magnifies the offset voltage. Obviously, the offset voltage of the opamp itself should be as low as possible.



Parts list
ADDRESS DECODER BOARD

Capacitors:
C_1 = 100n
C_2 = 22p
C_3 = 10μ; 10 V

Semiconductors:
IC_1 = 74HCT138
IC_2 = 74LS122

Miscellaneous:
K_1 = double-row 40-way right-angled header, or 40-way right-angled male header with ejector handles.
K_2 = double-row 26-way straight PCB header, PCB Type 880159 (see Readers Services page).

Fig. 10. Printed circuit board for the address decoder.

supply BS. The connection between pin 6 of K_2 and pin 19 of K_1 shows that we have opted for Port 1 line P1. Any other line is equally suitable, as long as the software for the I/O modules takes this into account.
If it is decided not to use the analogue output module, the last-mentioned link can be omitted. Similarly, the ±15 V supply is not required then.

The modules are ready after being assigned a memory address by placing a jumper on K_3.
There are only two, simple, adjustments to carry out on the analogue output board(s). First, correct the temperature coefficient of the LM336-2V5 by adjusting P_2 for a reference voltage of 2.490 V measured at pin 6 of the output connector, K_2. Next, write 1000_{10} to the DAC (10 mV/LSB) and set the full-scale output voltage to 10.00 V with the aid of P_1.

The I/O modules discussed have a relatively low current consumption, and are, therefore, conveniently powered from the existing supply for the BASIC computer. The analogue board draws about 10 mA, the digital board and the decoder each about 20 mA.

Final notes

The contents of the conversion register in the DAC1006 are not defined at power-on, so that the output voltage may not be nought then. When an XFER pulse is received by a DAC, all other DACs connected respond to this simultaneously. This means that the contents of the latches should correspond to the desired output voltage, which may not be the case at power-on.
The analogue and digital ground lines may only be connected on the address decoder board.

Table 2. Examples of elementary command routines

For analogue module:

```
100  E0 = 0F000H          REM output address (see K3)
110  XF = 0F700H          REM dummy address (transfer)
120   INPUT X             REM get byte to convert
130  X = X * 64           REM justify left
140  PORT1 = 1            REM write byte
150  XBY(E0) = X/256      REM i.e. MSB, and then
160  PORT1 = 0            REM LSB
170  XBY(E0) = X.AND.0FFH REM (only bits 6 et 7 are useful)
180 XBY(XF) = 0           REM clock 10-bit transfer
190 GOTO 120              REM end of loop
```

For digital module:

```
10 E1 = 0F100H       REM module address (see K3)
20 Y = XBY(E1)       REM read input byte from Y
30 XBY(E1) = 00F3H   REM write byte F3
```

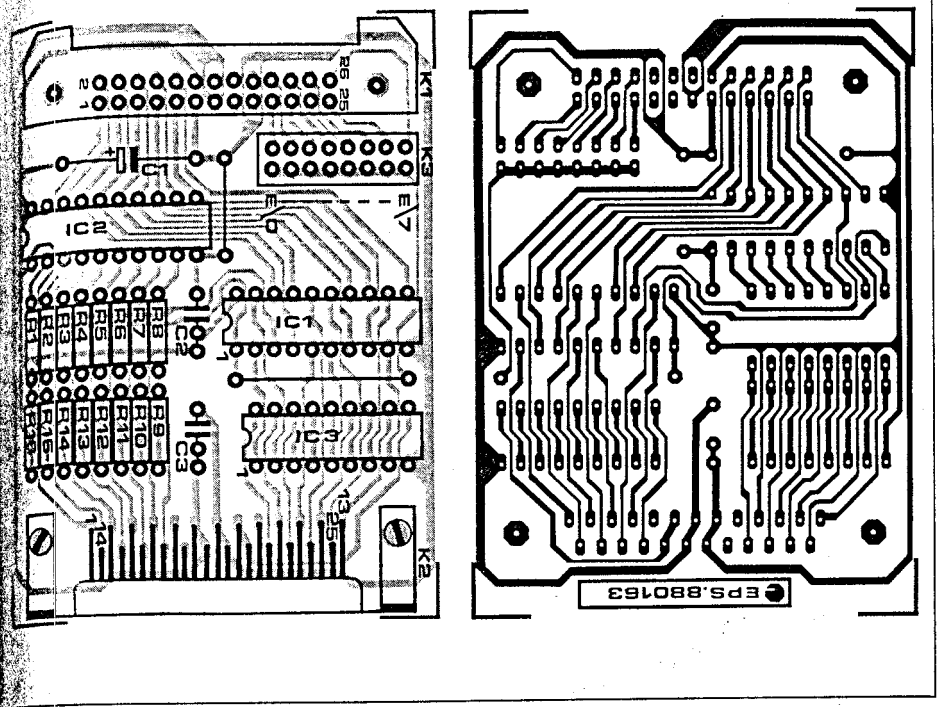


Fig. 11. Printed circuit board for the digital I/O module.

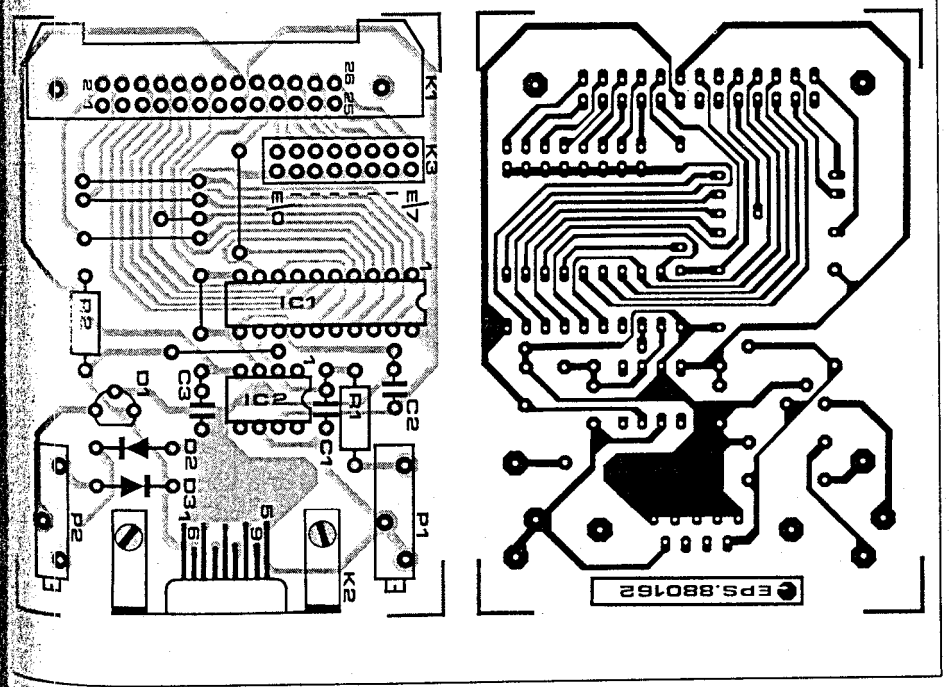


Fig. 12. Printed circuit board for the analogue output module.

When the logic outputs are used only for driving other digital circuits, the ULN2803 need not be fitted, and wire links may be installed between the PCB connections intended for the inputs and outputs of the chip.

Finally, do not forget that $\overline{E7}$ can not normally be used as a board selection signal because it is needed as XFER shared by the analogue output modules.

Reference:

(1) BASIC computer. *Elektor Electronics* November 1987, p. 24-31.

Parts list
DIGITAL I/O BOARD

Resistors:
R1 . . . R8 incl. = 100K
R9 . . . R16 incl. = 10K

Capacitors:
C1 = 10μ; 16 V
C2;C3 = 100n

Semiconductors:
IC1 = 74HCT377
IC2 = 74HCT541
IC3 = ULN2803A

Miscellaneous:
K1 = double-row 26-way right-angled header, or 26-way right-angled male header with eject handles.
K2 = 25-way D connector, male, with right-angled pins.
K3 = double-row 16-way straight PCB header.
1 jumper for mounting on K3.
PCB Type 880163 (see Readers Services page).

Parts list
ANALOGUE OUTPUT BOARD

Resistors:
R1 = 47K5 1%
R2 = 12K
P1 = 25K or 22K multiturn preset
P2 = 10K multiturn preset

Capacitors:
C1 = 1n0
C2;C3 = 100n

Semiconductors:
D1 = LM336-2V5
D2;D3 = 1N4148
IC1 = DAC1006 (National Semiconductor)
IC2 = OP-77 (PMI)

Miscellaneous:
K1 = double-row 26-way right-angled header, or 26-way right-angled male header with eject handles.
K2 = 9-way D connector, male, with right-angled pins.
K3 = double-row 16-way straight PCB header.
1 jumper for mounting on K3.
PCB Type 880162 (see Readers Services page).