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6809 DRAM controller

This circuit of a Random Access Memory controller is a real treat for owners of a 6809. It enables at least 128 k bytes of a dynamic RAM to be addressed and even then it has some spare capacity.

The controller cannot be used for chips other than the 6809 as it makes use of a special feature of that particular processor. The memory refresh is produced by timing signals from the microprocessor E and Q. An OR function with these two signals is performed by gates N2, N3 and N10, and the timing diagram is shown in figure 3. The circuit of figure 1 shows only two of the eight memory ICs (4164); the corresponding signals must, of course, be fed to each of the eight memories of a 64 k block (see figure 2). A buffer for the data bus is not envisaged; if this is desired, take care that is operating speed is sufficient, otherwise it could upset the operation of the controller.

By 'ANDing' the E and $\overline{Q}$ signals, the $\overline{CAS}$ signal for both 64 k stacks is produced. The $\overline{CAS1}$ select signal for the upper 64 k stack is produced by 'NANDing' $\overline{CAS}$ and the 1Y output of IC5; that for the lower 64 k ($\overline{CAS2}$) stack by 'NANDing' $\overline{CAS}$ and output 2Y of IC6. The software should ensure that during the row address time suitable signals (A0, A1, A2, A14 and A15) for driving IC6 and IC7 are present on the address bus.

It is almost impossible to show this correlation clearly, but the matter should be much more obvious if you imagine IC7 as being replaced by the four bistables which make it up.

A final note: IC6 produces the MSB (address 15) at its 3Y output when strobed by the signal on address bus line A15.

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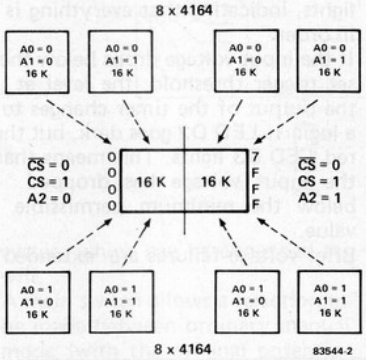

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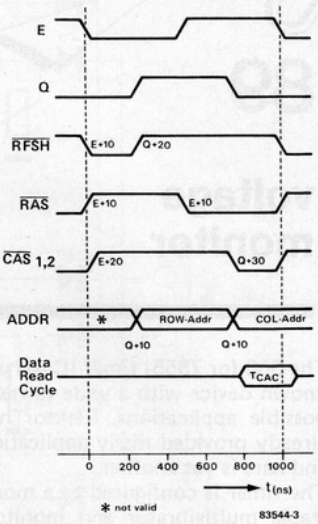

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