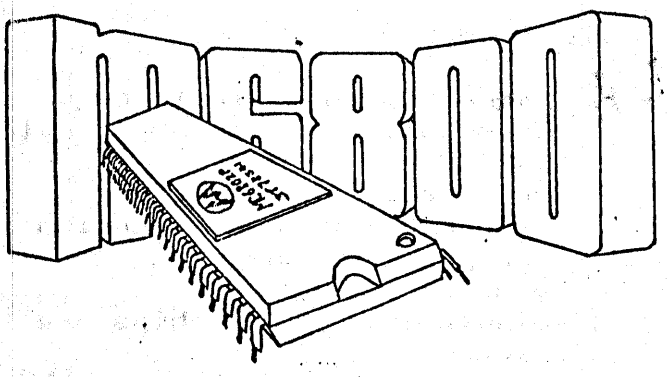

MICROPHILE

Jonathan Eva , Neil Walsh

This month we are devoting 6800 Microphile to a brief description of the C3Bus, the 680X Group and a specification of the Group's 6809 microsystem as we feel it will be of interest to our new readers.

THE C3BUS - A BRIEF DESCRIPTION

Introduction

The C3Bus is a microcomputer bus system originally developed by the Committee of the Cape Computer Club and subsequently revised by the 680X Group of the Cape Computer Club to allow the easy use of Motorola 6800 family devices with this bus. It is based on the standard 114,3 x 203,2mm Verocard with a 42-way keyed edge connector.

An informal description of the bus signals is given below.

1 - +5V Power supply
2 - -5V Power supply
3 - +12V Power supply
4 - -12V Power supply
5 - Reset. Open collector, active low to reset all devices
6 - Clock(E). 1 MHz square wave.

KEY

8-
23 - A0 to A15. Address lines, tristated during HALT.
24 - Wait. Open collector, active low to extend memory access for slow devices.
25-
32 - D0 to D7. Data lines, tristated during HALT.
33 - Halt. Open collector, active low to halt the CPU.
34 - Bus Available. Active low, indicates that the CPU is halted and address, data and control busses are tristate.
35 - Valid Memory Address (A17). Active high, indicates that a valid memory access is taking place. When the bus is connected for addressing 256K, this line becomes A17. Tristated during HALT.
36 - Non Maskable Interrupt. Open collector, active low.
37 - Interrupt Request. Open collector, active low maskable interrupt.
38 - Read Strobe. Active low during the second half (E high) of each valid read memory cycle. Tristated during HALT.
39 - Write Strobe. Active low during the second half of each valid memory write cycle. Tristated during HALT.
40 - I/O Select (A16). Active low, indicates that the current memory access is taking place within a defined 256-byte memory block used for I/O purposes. When the bus is connected to address 256K, this line becomes A16. Tristated during HALT.
41 - Read/Write. High to indicate that the current memory access is a read, low to indicate a write. Tristated during HALT.
42-
43 - Ground.

THE 680X GROUP

The 680X group of the Cape Computer Club is a group of about eight people who either own, or are in the process of acquiring, personal computers based on the 6802 or 6809 processors. These computers are made up of a number of printed circuit boards based on the C3Bus (see preceding column) and are designed and financed solely by the group.

The cards successfully produced by the group to date are listed below, together with their main features. It can be seen that the complete system forms a computer of great power and flexibility. It will operate successfully under the Technical Systems Consultants FLEX Operating System, and the prototype system is running the STYLOGRAPH Word Processor and 8080, Z80 and 6502 Cross-Assembler packages. Additional software in the form of powerful utility programs, high and low level languages and of course the ubiquitous games programs is readily available or is being created at the moment, making this system the ideal home computer with the flexibility to adapt to almost any computing requirement.

6809 MICROSYSTEM
SPECIFICATIONS

CPU MODULE

1. 6809 Microprocessor - 1 MHz
2. 4K/2K on-board monitor (2732/2716)
3. Dynamic Address Transfer in 4K blocks
4. 256K byte memory map (or 64K map selectable)
5. 256 byte I/O page switch selectable
6. Interrupt or Fast Interrupt switch selectable
7. Power-on reset
8. Single +5 Volt operation

RAM MODULE

1. 64K bytes on a single card
2. Expandable to 256K bytes using 64K IC's
3. No circuit modifications required for 256K expansion
4. Low power consumption - Dynamic memory
5. Single +5V if 64K chips are used
6. 4 banks individually enabled or disabled by switches

PARALLEL PORT BOARD

1. 4 x 6821 PIA ports
2. Total of 80 interface lines
3. Large wire wrap prototyping area
4. Optional on board real time Calendar/Clock chip
5. Battery backup for clock
6. Selectable interrupt lines to CPU
7. 4 selectable interrupt rates from real time clock
8. Card address switch selectable

SERIAL PORT BOARD

1. 2 x 6850 ACIA serial ports
2. Baud rates of ports individually software selectable
3. On board switch selector for power-on baud rate initialisation
4. User programmable 16 bit counter/timer for multi-tasking or timing applications
5. Card address switch selectable
6. One port is RS232 level buffered
7. One port selectable for RS232/TTL buffered

FLOPPY DISK CONTROLLER

1. 5 1/4" single/double density
2. Density software selectable
3. On board drive select logic for up to four drives
4. Optional side selection
5. Phase lock loop data recovery
6. Write precompensation logic

7 Western Digital Controller chips
8 Inactivity motor switch
9 Card address switch selectable
10 Extended Bus master I/O selection
11 Standard SHUGART connection

VDU CONTROLLER

1 6845 CRT controller chip
2 Transparent access to all screen RAM at full CPU speed
3 64K Effective Address Transfer
4 4K of Text RAM (two full screen pages)
5 4K character generator RAM for character font changes or low resolution graphics
6 On board attribute register allowing underlining, blinking, reverse video, intensity control and eight colours
7 Software dot frequency selection to cater for change of character size
8 Software dot format selection - 7x9 or 5x7
9 Characters per line and rows per screen programmable via 6845
10 On board timing and logic to allow for access of external 16K high resolution RAM
11 Optional high resolution graphics using additional expansion memory board
12 Optional high resolution colour graphics using further expansion memory boards
13 Both high resolution/low resolution (text) displays will automatically overlay each other
14 Display of graphics can be switched on or off under software control
15 Nominal dot frequency 12 MHz although lower frequencies can be used by reducing the screen character or dot format.

FIRMWARE MONITOR

1 Fast and versatile screen handling output routines facilitating programmable characters per line, lines per screen and page select. These are parameter driven from memory tables which can be altered by the user at any time
2 Command Line Editor - a powerful keyboard input routine which allows keyboard entry of a string of characters to a memory buffer which when terminated with a CR will return these characters to the system input routine each time it is called. The editor features backspacing, cursor left or right, overwriting, inserting or deleting characters, or returning the last entered line again for re-editing if the line was returned to the system with an error.
3 Normal monitor commands which include a powerful screen based memory examine/change command which allows the altering of hex codes or text in memory and makes it possible to scan through memory at an exceptional pace.
4 Automatic setting up of the CRTC contoller and screen memory.
5 Automatic setting up of the Dynamic Address Transfer registers on the CPU
6 Automatic setting up of the serial port baud rates according to a selector switch on the serial card.
7 Disk booting or quick loading of the system image.
8 SWTPC and TSC compatibility.