MOTOROLA

M68MEB1

MICROPROCESSOR EVALUATION BOARD

The M68MEB1 Evaluation Board provides the user with a quick and efficient means to evaluate the operating characteristics of the M6800 family of Parts.
The on-board crystal controlled clock circuit provides the module with the capability of working with dynamic memories and slow memories. The clock circuit also generates the basic timing signal used by the module's baud rate generator.
The Microprocessor Evaluation Board interfaces directly with either a TTY (20 mA current loop), a TTL or a RS232-C compatible terminal providing direct communication with the module's MINI-BUG II Firmware.

The MEB consists of:
1 M68SAC1 Stand-Alone Computer
1 MEC68MIN2 Minibug II Firmware ROM

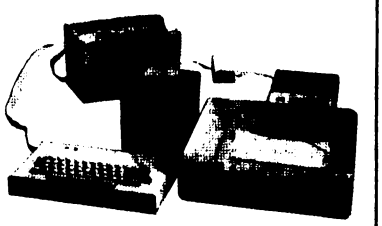
- Four 8-bit parallel Input/Output Ports and Control Lines for Peripheral Interfacing
- Two asynchronous Input/Output Ports with one RS232.C/TTL/TTY Current-Loop interface
- 384 bytes of RAM
- Three MCM68708 or equivalent AROM/ROM sockets
- One MCM6830 Minibug II Firmware ROM
- 921.6 KHz on-board crystal controlled clock generator
- Fully buffered Three-State Bus Connector
- Bus DMA Capability
- Fully compatible with all EXORciser modules

By adding options, the Microprocessor Evaluation Board can be upgraded to an Autonomous Development System.

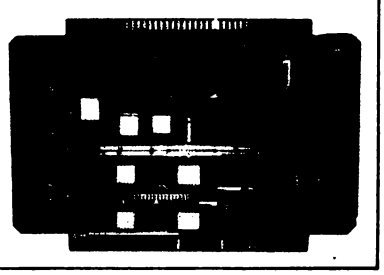
POLYVALENT DEVELOPMENT SYSTEM

MICROPROCESSOR EVALUATION BOARD

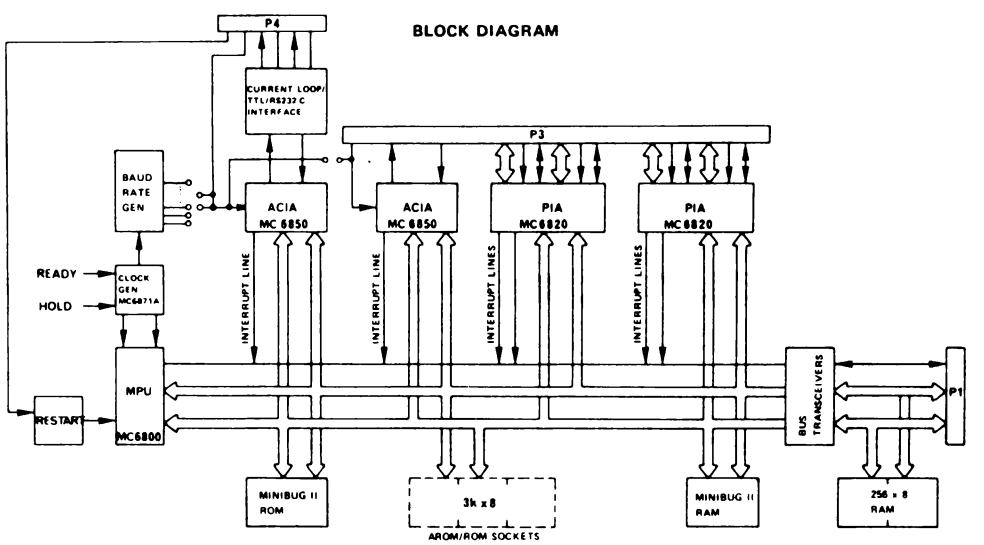
PDS



MEB



BLOCK DIAGRAM



MODULE SPECIFICATIONS

Specification		Value
Memory Size Capability		65, 536 bytes maximum.
On-Board Memory Size		384 bytes of RAM 3 x 1 K-byte MCM68708 compatible AROM/ROM Sockets 1 x 1 K-byte MCM6830 MINIBUG II ROM
Memory locations available for external expansion		44 K-byte: 0000 to 7FFF 9000 to 9FFF B000 to CFFF
Word Size	Data Address Instruction	8 bits 16 bits 8, 16, or 24 bits
Instruction Set		72 variable length instructions
Interrupts		Maskable and non-maskable real-time interrupts; Software interrupt
Clock Signal		921.6 KHz
Address Bus Data Bus Control Bus		Three-state TTL voltage compatible Three-state TTL voltage compatible TTL voltage compatible
MC6820 Peripheral Interface Adapter Lines MC6850 Asynchronous Communication Interface Adapter Serial Transfer Rate Terminal interface		TTL voltage compatible* TTL voltage compatible* 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, 9600 baud RS232.C, TTL or 20 mA Current-Loop
Power requirements		+ 5 Vdc at 1,5 A + 12 Vdc at 200 mA − 12 Vdc at 200 mA − 5 Vdc on board converter
Operating temperature		0° to 70 °C
Dimensions Width Height Thickness PC Board Thickness		 248 mm 9.75 in. 165 mm 6.5 in. 13 mm 0.5 in. 1.6 mm 0.062 in.

*See MC6820 and MC6850 data sheets for specifications on these signals.

Minibug II Firmware Features

MEC68MIN2 ROM
MEC68MIN21 Listing

The Minibug II Firmware provides the user with an efficient means to debug his program. It communicates with a serial peripheral (which can be the IOS ACIA) through an ACIA located in 8008 and works with either 1 or 2 stop bits.

Memory Load	L
Load Binary object tape	Z
Print/Punch Dumps (from vect. A002/A003 to vect. A004/A005).	P
Punch Binary object tape (from vect. A002/A003 to vect. A004/A005)	Y
Memory Examine/Change	M nnnn
– open next location	(LF)
– open previous location	↑
Print MPU Registers (CC, B, A, X, PC, SP) (saved in stack vect. A008/A009)	R
Go to user's program	G nnnn
Memory test function (from vect. A002/A003 to vect. A004/A005)	W
Select 2 stop bits (default value)	S1 (for Speed 110 baud)
Select 1 stop bit	S3 (for Speed ⩾ 300 baud)
ROM address	E000 to E3FF
RAM address	A000 to A07F
ACIA address	8008
User's stack pointer	saved
Space required in user's stack	14 bytes
Restart Vector	ROM* (E3FE/E3FF)
NMI Apparent Vector	RAM* (A006/A007)
SWI Apparent Vector	RAM* (A00A/A00B)
IRQ Apparent Vector	RAM* (A000/A001)

*The actual vectors are fetched in ROM, but then, MINIBUG II fetches the apparent NMI, SWI and IRQ vectors in RAM and jumps to the corresponding user's service routine.
To access its ROM vectors, the MINIBUG II ROM should be accessed with the following address patterns:

1110 00XX XXXX XXXX
or 1111 . XX XXXX XXXX

The SWI apparent vector (RAM A00A/A00B) is initialized at E227 (SWI Breakpoint MINIBUG II Routine) each time a Reset is applied.