



MOTOROLA

**M68ADS.
M68ADW.**

AUTONOMOUS DEVELOPMENT SYSTEM

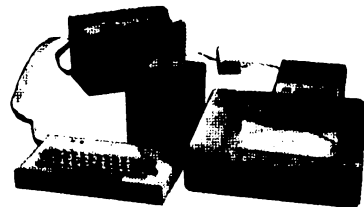
The M68ADS. is a complete development system including facilities for developing a hardware/software design and provides a very cost effective CRT terminal capability that avoids the use of the noisy and slow teletypewriter. The Autonomous Development System consists of:

- 1 M68MEB1 Microprocessor Evaluation Board which includes:
 - 1 M68SAC1 Stand Alone Computer
 - 1 MEC68MIN2 MINIBUG II Firmware
- 1 M68DIM Display Interface Module
- 1 M68MDM1 5" Display Monitor
- 1 M68IOS1 Input/Output Supervisor Firmware
- 1 M68KBD1 Full ASCII Keyboard
- 1 M68ICC1 Interconnection Cables Set
- 1 M68BSC1 Bus System Card

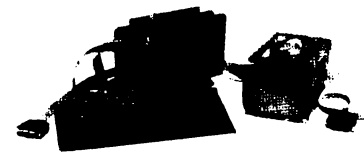
The M68ADS. can be used as a complete development system with full MINIBUG II and IOS firmware capability or as a multi-terminal for the EXORciser. These configurations are switch selectable.

**POLYVALENT DEVELOPMENT SYSTEM
AUTONOMOUS DEVELOPMENT
SYSTEMS**

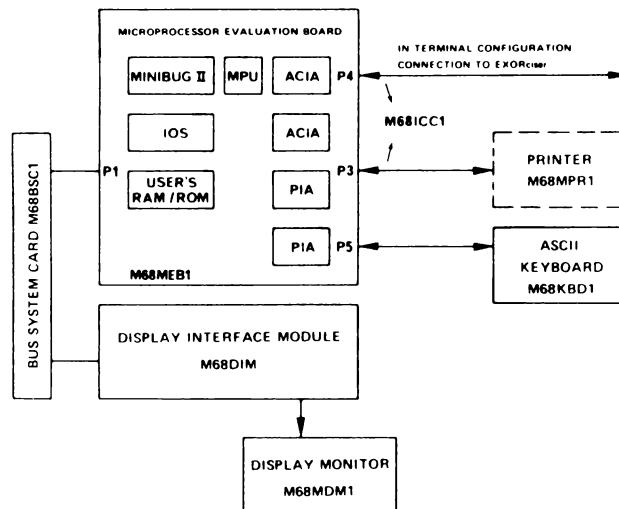
PDS



M68ADS.



BLOCK DIAGRAM



MINIBUG II FIRMWARE FEATURES

MEC68MIN2 ROM
MEC68MIN21 Listing

The Minibug II Firmware provides the user with an efficient means to debug his program. It communicates with a serial peripheral (which can be the IOS ACIA) through an ACIA located in 8008 and works with either 1 or 2 stop bits.

Memory Load	L
Load Binary object tape	Z
Print/Punch Dumps (from vect. A002/A003 to vect. A004/A005).	P
Punch Binary object tape (from vect. A002/A003 to vect. A004/A005)	Y
Memory Examine/Change	M nnnn
– open next location	(LF)
– open previous location	↑
Print MPU Registers (CC, B, A, X, PC, SP) (saved in stack vect. A008/A009)	R
Go to user's program	G nnnn
Memory test function (from vect. A002/A003 to vect. A004/A005)	W
Select 2 stop bits (default value)	S1 (for Speed 110 baud)
Select 1 stop bit	S3 (for Speed ≥ 300 baud)
ROM address	E000 to E3FF
RAM address	A000 to A07F
ACIA address	8008
User's stack pointer	saved
Space required in user's stack	14 bytes
Restart Vector	ROM* (E3FE/E3FF)
NMI Apparent Vector	RAM* (A006/A007)
SWI Apparent Vector	RAM* (A00A/A00B)
IRQ Apparent Vector	RAM* (A000/A001)

*1 If the MINIBUG II is used in conjunction with IOS Firmware, the actual vectors are fetched in IOS ROM, but after IOS service, control is given to MINIBUG II which fetches the apparent NMI, SWI and IRQ vectors in RAM and jumps to the corresponding user's service routine. The MINIBUG II ROM should be accessed with the following address pattern

1110 00XX XXXX XXXX

2. If the MINIBUG II ACIA (8008) is directly connected to a serial terminal and the IOS Firmware is not present, the actual vectors are fetched in MINIBUG ROM, but then, MINIBUG II fetches the apparent NMI, SWI and IRQ vectors in RAM and jumps to the corresponding user's service routine. The MINIBUG II ROM should be accessed with the following address patterns

1110 00XX XXXX XXXX
or 1111 XX XXXX XXXX



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Co-resident configuration

The co-resident software MINIBUG II and the user's program communicates with IOS Firmware through the IOS ACIA located at 8010.

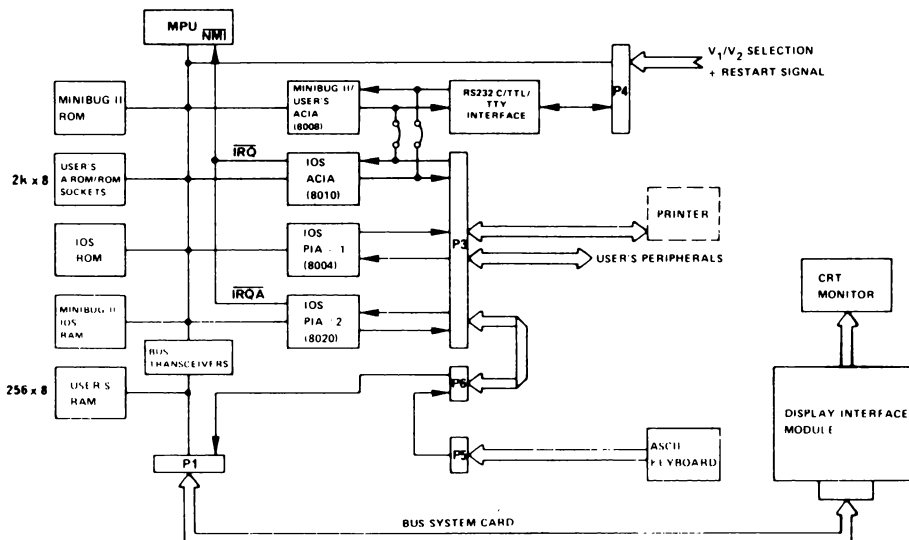
The IOS routines are accessed by NON MASKABLE INTERRUPTS generated by its interfaces. If another source generated the NMI, IOS gives control back to E005 location, which is the MINIBUG II NMI service routine.

– If a character was received in the IOS ACIA (8010) coming from the user's/MINIBUG II ACIA (8008) it is transmitted to the Printer PIA (8004) and to the Display Interface Module. The non-visible characters are not transmitted.

– If a character was received in the Keyboard PIA (8020), it is transmitted to the IOS ACIA (8010), in order to be received later on in the user's/MINIBUG II ACIA (8008). If CtrlE (Erase screen) or CtrlB (Background Change for subsequent characters) were received from the Keyboard, they are not transmitted to the ACIA.

IOS ROM address	DC00 to DFFF*
IOS RAM address	A000 to A07F shared with MINIBUG II Firmware
IOS ACIA address	8010
Printer PIA address	8004
Keyboard PIA address	8020 (PA0 to PA6)
Bell line	CA2 of PIA (8020)
Hardware Top-of-Page line pointer PIA address	8022
User's Stack Pointer	Saved
Space required in user's stack	28 bytes
Restart action	initializes IOS interfaces, jumps to MINIBUG Restart Routine
NMI action	IOS action and jumps to MINIBUG NMI Routine
SWI, IRQ action	jumps to MINIBUG SWI, IRQ Routine
Start up action	Erases screen, Restart

*The ROM should be wired with the following address patterns:
1101 11XX XXXX XXXX
or 1111 ..XX XXXX XXXX



M68ADS. ● M68ADW.

Terminal Configuration

The external system, as the EXORciser, communicates with the IOS Firmware through ACIA located at 8008.

The characters to be printed are stored in a buffer of 123 characters, which is sent to the printer when full or at least each 300 ms without receiving a new character from the terminal ACIA. The PA7 line of the PIA (8020) is pulled high during Printer Operation. This line should be connected to the CTS line of the main system ACIA (i.e. DEBUG ACIA) in order to inhibit the transmission of new characters.

The Keyboard accesses to IOS routines by generating a NON MASKABLE INTERRUPT.

Two modes of operation are possible:

Local mode (Off-Line)

- The ACIA (8008) is not taken into account.
- The characters received from the Keyboard PIA (8020) are transmitted to the Display Interface Module and to the Printer Buffer. The non-visible characters are not transmitted.

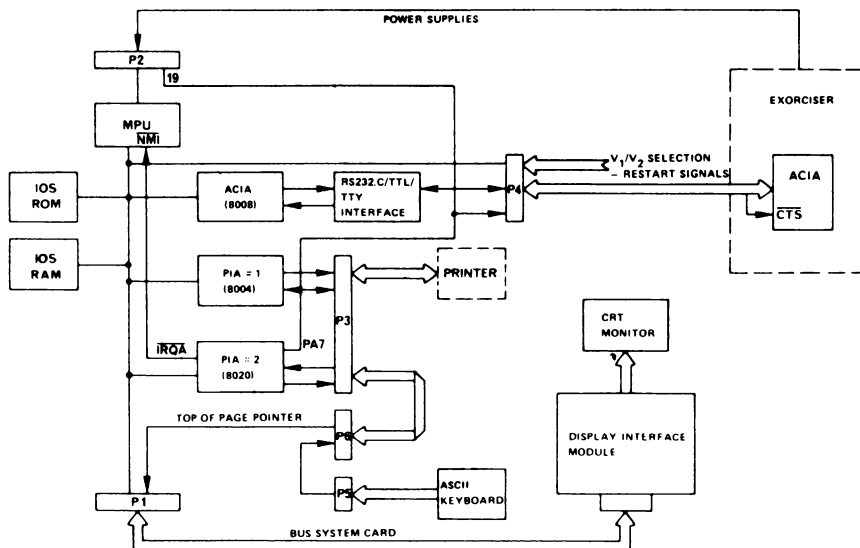
On-Line mode (full-duplex)

- The characters received from the ACIA (8008) are transmitted to the Display Interface Module and to the Printer Buffer. The non-visible characters are not transmitted.
- The characters received from the Keyboard PIA (8020) are transmitted to the ACIA (8008). All characters, except CtrlB, CtrlE and CtrlO are transmitted.

ROM address	DC00 to DFFF*
RAM address:	
scratch pad	A000 to A07F
Printer Buffer	0000 to 007F
ACIA address	8008
Printer PIA address	8004
Keyboard PIA address	8020 (PA0 to PA6)
Bell line	CA2 of PIA (8020)
Hardware Top-of-Page line	
pointer PIA address	8022
CTS line	PA7 of PIA 8020

* The ROM should be wired with the following address pattern,
1101 11XX XXXX XXXX
or 1111 ..XX XXXX XXXX¹

¹Note: in this configuration, A9 is set to 0 by hardware when the MPU accesses to FFF8 to FFFF vectors.



MOTOROLA Semiconductor Products Inc.

INPUT/OUTPUT SUPERVISOR

The M68IOS1 Input/Output Supervisor Firmware provides the user with an efficient means to interface the Polyvalent Development System Peripherals (CRT, Keyboard, Printer) to either a co-resident MINIBUG Firmware and a user's software or to an external asynchronous line such as the TTY connection of the EXORciser.

- Compatible with M68DIM1 and M68DIM2 16-line x 32-character Display Interfaces
- Compatible with M68DIM6 16-line x 64-character Display Interface
- Can work with co-resident standard I/O routines
- Standard ACIA main system connection (8-bit word, 1 stop bit)
- Cursor control
- Background control (white-on-black or black-on-white display).

When the display page is full, the next line will be displayed at the bottom line, and the whole page is shifted one line up, losing the top line (Scroll-up Display).

IOS CONTROL CHARACTERS

Code	Effect	Co-resident configuration received by		Terminal configuration		
		Keyboard	ACIA (8010)	Off-line received by Keyboard	On-line received by	
					Keyboard	ACIA (8008)
CtrlE	Erase screen	X	X	X	X	X
CtrlB	Background change for subsequent characters	X	X	X	X	X
CtrlO	Change mode of Operation (local/on-line)	-	-	X	X	X
CtrlG	Sound the bell (negative pulse on CA2 of PIA 8020)	-	X	X	-	X
CtrlU	Cursor Up one line	-	X	X	-	X
CtrlW	Cursor doWn one line	-	X	X	-	X
CtrlN	Cursor to Next character	-	X	X	-	X
CtrlH	Cursor to previous character (Back Space)	-	X	X	-	X
CtrlL	Cursor to home (Form-Feed)	-	X	X	-	X
CtrlC	Clear page from cursor	-	X	X	-	X
CtrlK	Kill line from cursor	-	X	X	-	X
Null	Not transmitted	-	X	X	-	X
Rubout	Not transmitted	-	X	X	-	X



ORDERING INFORMATION

OPTION	DESCRIPTION
M68ADS1	completely assembled and tested system, with a 5" CRT 16-line x 32-character Display
M68ADS6	completely assembled and tested system, with a 5" CRT 16-line x 64-character Display
M68ADW1	completely assembled and tested system, with 16-line x 32-character Interface, without CRT-monitor (for use with a standard TV-receiver, VHF, 55.25 MHz channel E3)
M68ADW2	completely assembled and tested system, with 16-line x 32-character Interface, without CRT-monitor (for use with a standard TV-receiver, UHF, 591.25 MHz, channel E36)
M68ADW6	completely assembled and tested system, with 16-line x 64-character Interface, without CRT-monitor (for use with a M68MDM9 9" CRT-monitor)

ACCESSORIES	DESCRIPTION
M68MDM9	9" CRT-monitor
M68MPR1	Motorola 30 chr/sec. Printer
M68MPP1	Electro-sensitive paper for MPR Printer
M68DMC1	Display Monitor Cabinet for 5" CRT Monitor
M68DMC9	Display Monitor Cabinet for 9" CRT Monitor
M68KBC1	Keyboard Cabinet for M68KBD1
M68EAM1	ROM resident Assembler/Editor Module
M68EAB1	ROM resident Assembler/Editor/BASIC Interpreter Module
MMS68103	16K-byte RAM module
MMS68103-1	8K-byte RAM module
M68CIM1	Audio Cassette Interface Module
M68PPR2	PDS PROM Programmer
M68MMLC2	Chassis with 10-slot card-cage and power-supply
M68MMSC2	Chassis with 5-slot card-cage and power-supply
M68MMCC05	5-slot card-cage
M68MMCC10	10-slot card-cage
MEC68MIN3E	MINIBUG 3E Firmware ROM, with Breakpoints capability.

